Amendments to the Claims

1. (Original) A computing system, comprising:

a plurality of pipelined processors, each processor having a power dissipation controller for variably controlling internally generated power dissipation to a capacitive model which achieves substantially maximum average power output dissipation relative to throttled instruction input rate; and

a cooler for cooling the system relative to power dissipated from the processors.

2. (Original) A system of claim 1, further comprising operating system software for specifying constants within register memory within the controller, the constants forming the capacitive model.

3. (Original) A system of claim 1, wherein the controller inserts a lp-bit to one or more stage execution circuits within the processor in order to stall high powered instructions through a pipeline.

4. (Original) A system of claim 1, wherein each processor further comprises at least one additional power dissipation controller for controlling processing in different pipelines.

5. (Currently Amended) A pipelined processor of the type having at least one register pipeline, comprising:

a power dissipation controller for stalling instructions to control average power dissipation of the pipelined processor; ~~and~~

logic for comparing a threshold to current capacity representative of a thermal response of the pipelined processor and for implementing a lower power state within the register pipeline of the pipelined processor when the capacity exceeds the threshold; and

register memory for storing constants of capacitive feedback.

6. (Canceled)

7. (Currently Amended) The pipelined processor of claim [[6]] 5, the constants being written to the register memory and including a bleed rate, one or more issue weights, and the threshold.

8. (Previously Presented) The pipelined processor of claim 7, the logic computing current capacity as a number of issued instructions multiplied by the issue weights and subtracted by the bleed rate.

9. (Original) The pipelined processor of claim 8, the issue weights corresponding to relative power dissipation, wherein issue weights for higher power instructions are greater than issue weights for lower power instructions.

10. (Original) The pipelined processor of claim 5, the power dissipation controller inserting a low power operation to the register pipeline to stall the instructions.

11. (Previously Presented) A power dissipation controller for controlling power dissipation within a pipelined processor, comprising:

a register access bus for setting a bleed rate;

logic for multiplying each instruction of the pipelined processor by an issue weight; and

logic for stalling instructions of the pipelined processor when capacity of the pipelined processor exceeds a threshold, wherein the capacity is determined as being (a) reduced by the bleed rate and (b) increased by the instruction multiplied by the issue weight.